

GA-F2A68HM-S1

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APU_VDDIO_SUS=DDR15V

APU_VTT_SUS=DDRVTT

APU_VDDP_RUN=APU_VDDR_RUN=APU_VDDP

+1.1V_RUN=FCH_VDD_11_RUN=VCC_SB

+3.3V_RUN=VCC3

+3.3V_ALW=3VDUAL

GIGABYTE™

Title

COVER SHEET

Size

Custom

Document Number

GA-F2A68HM-S1

Rev

1.1

Date:

Wednesday, December 17, 2014

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25

Model Name:GA-F2A68HM-S1


Component value change history

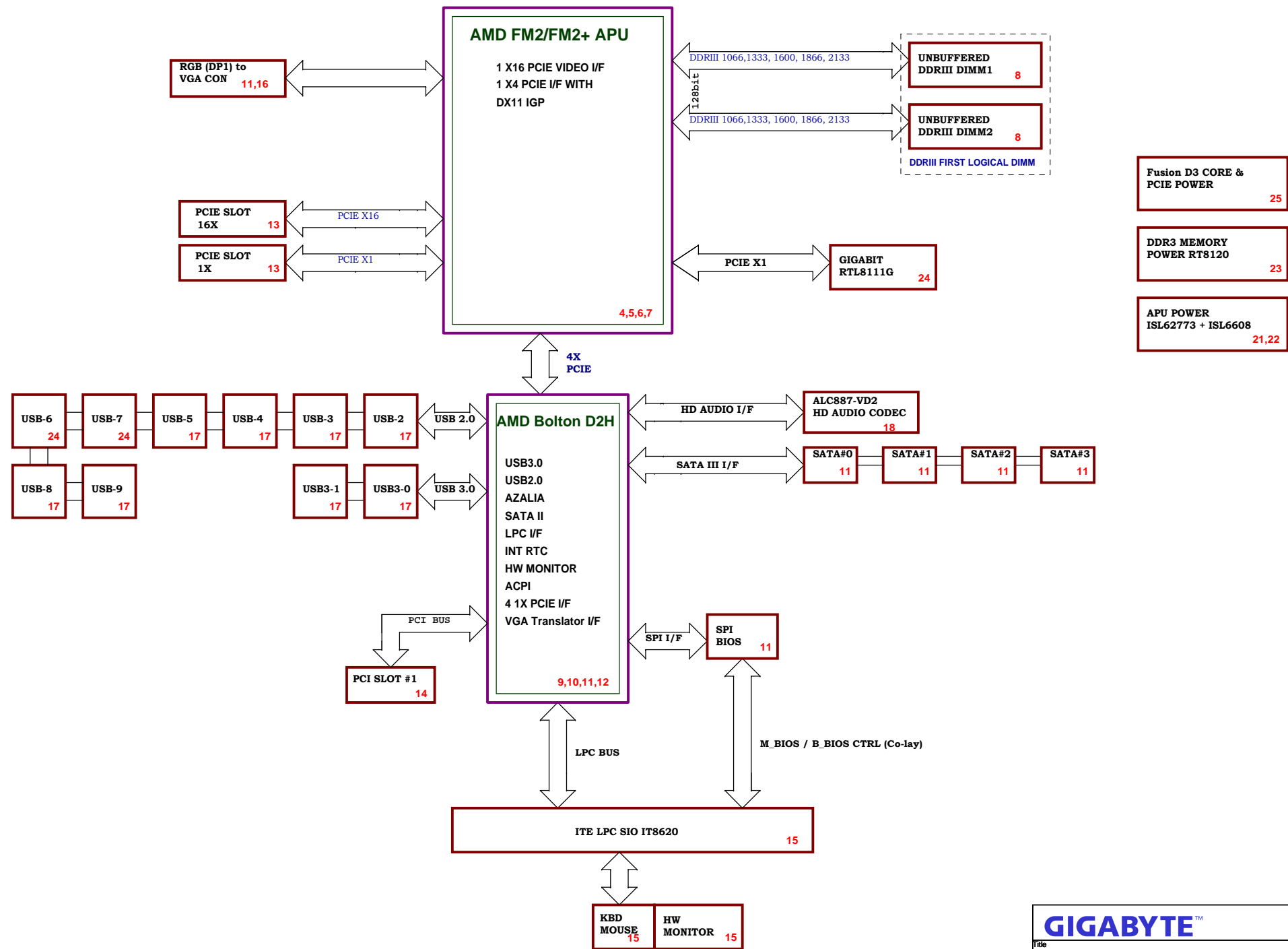
Version: 1.1
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P-Code:

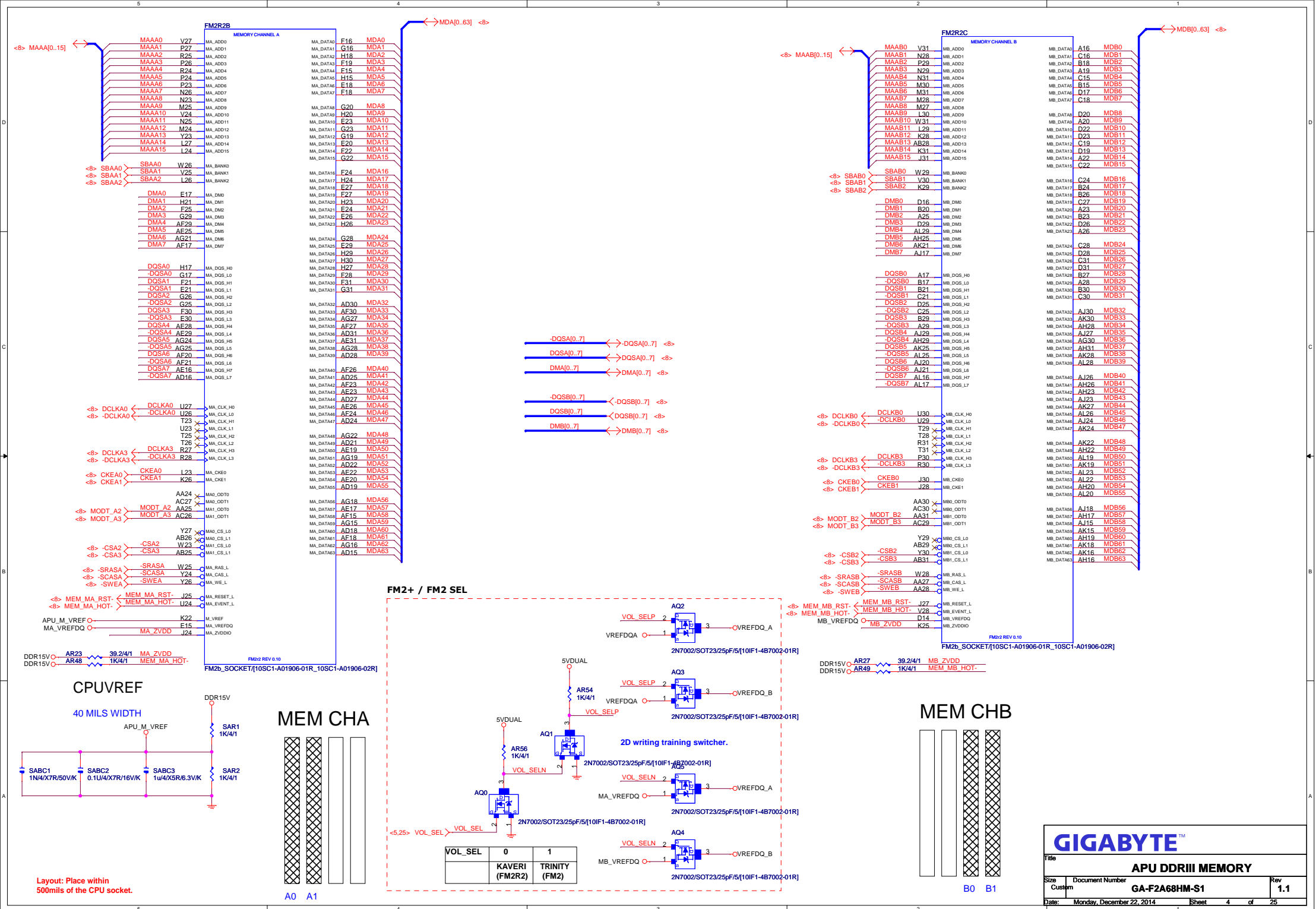
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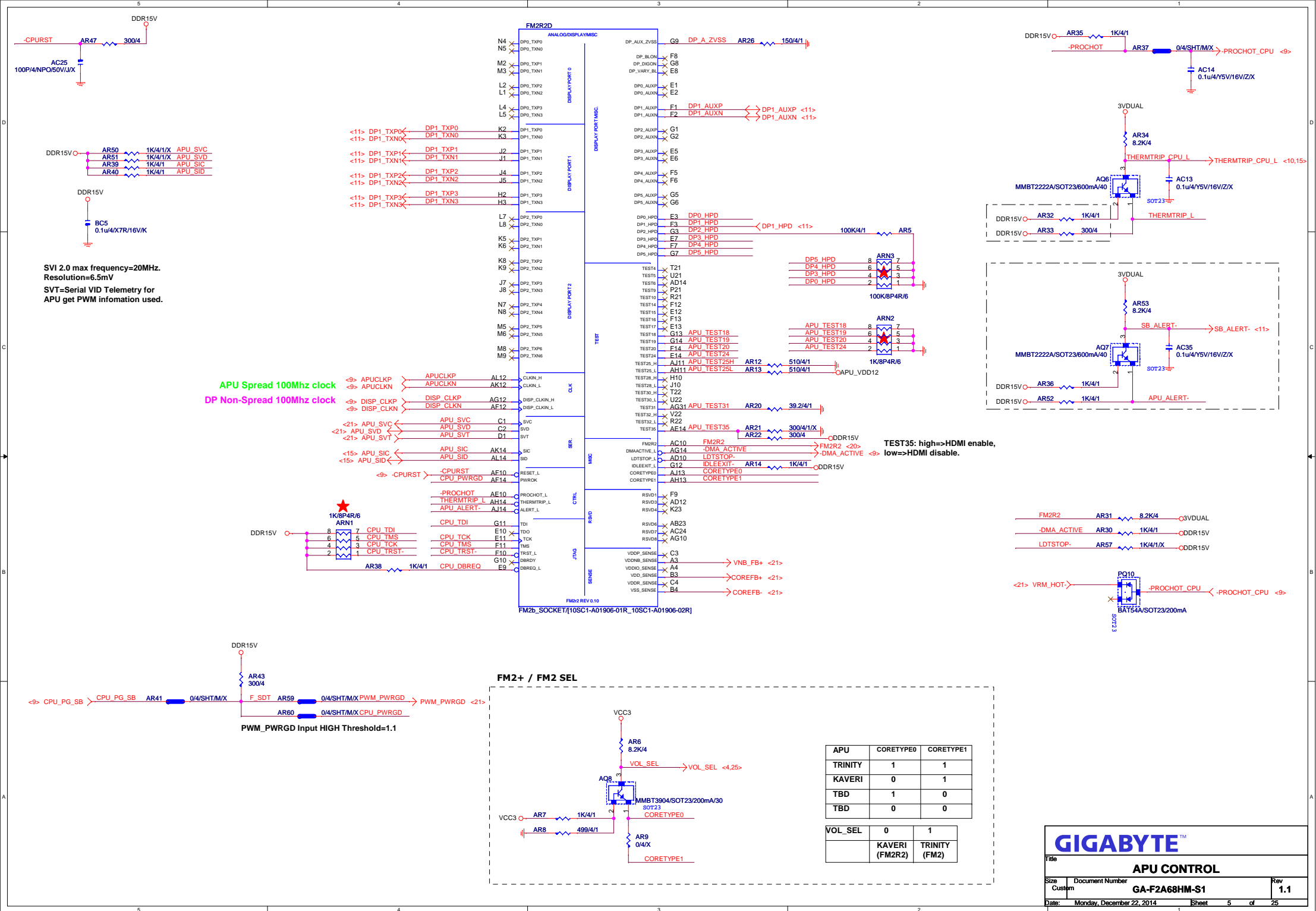
Circuit or PCB layout change for next version

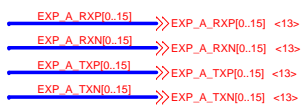
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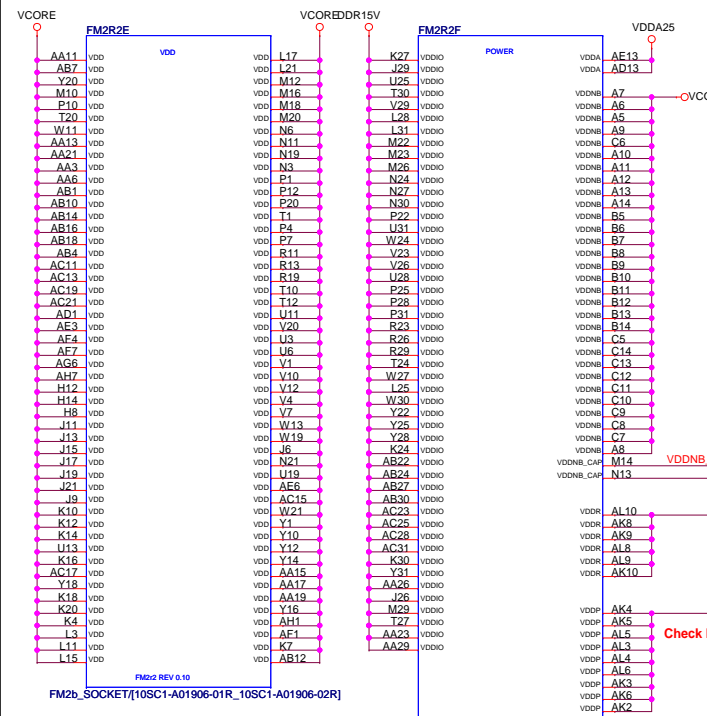




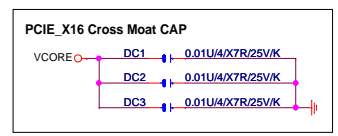
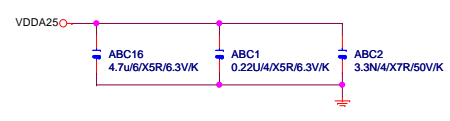




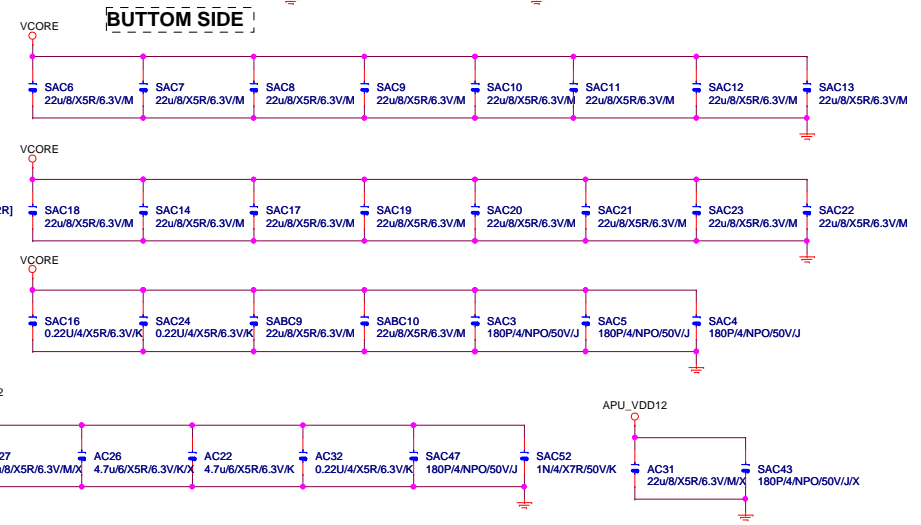
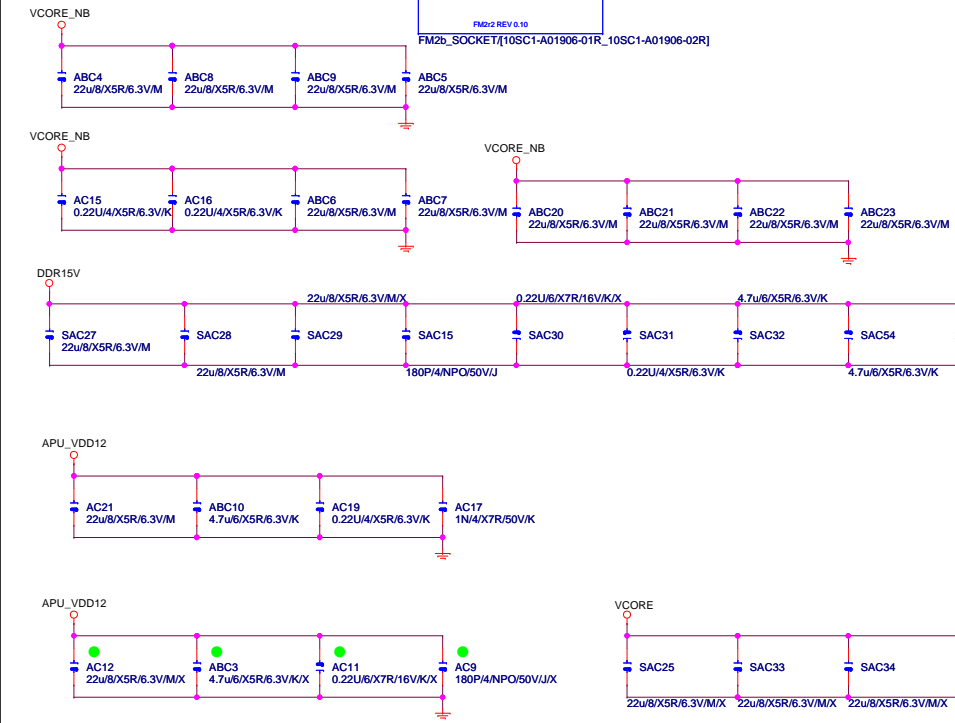
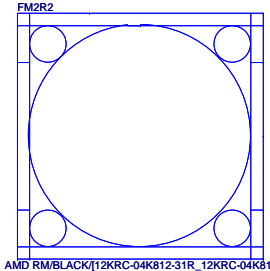
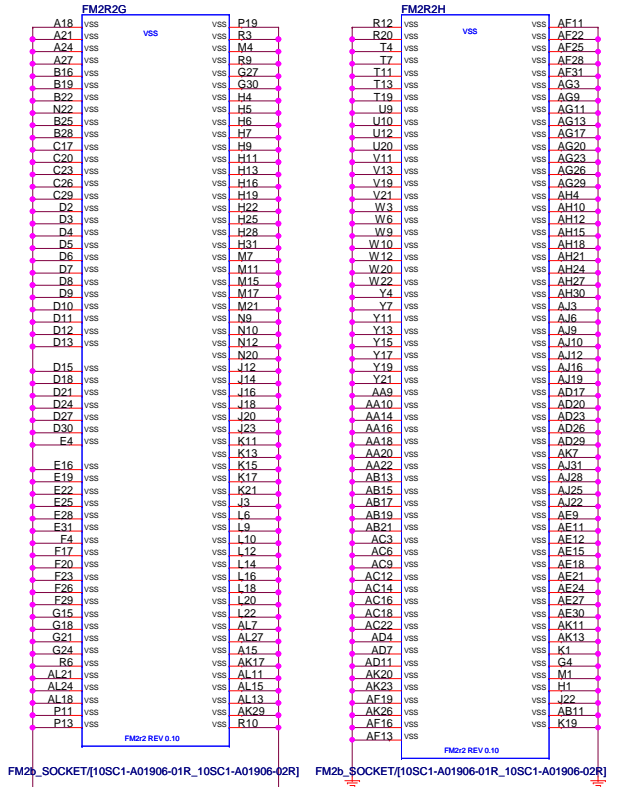
DDR15V=1.25V/1.35V/1.5V(DDR3)



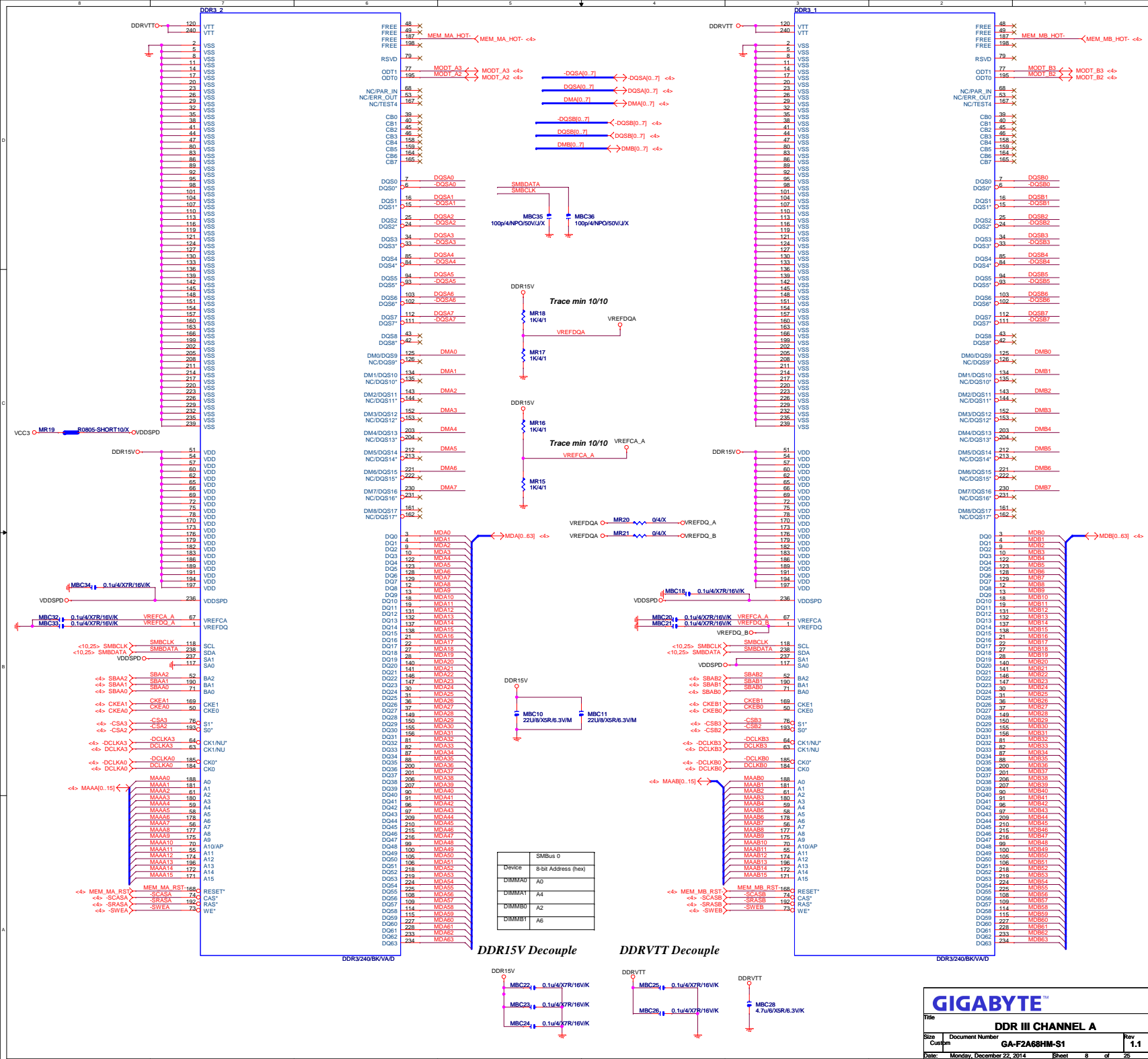
GND:232 pin,
VCORE:99 pin,
VCORE_NB: 30 pin,
DDR15V:49 pin,
VDDP:9 pin, VDDR:9 pin,
VDDA25:2 pin,
VDDNB_CAP:2 pin,
Total:430 pin.



Place close N13, M14 pin inside the backplate cavity opening.

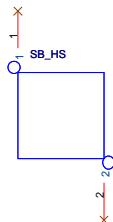


GIGABYTE™			
Title APU POWER & GND			
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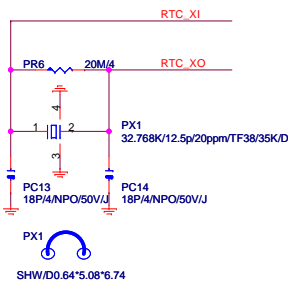




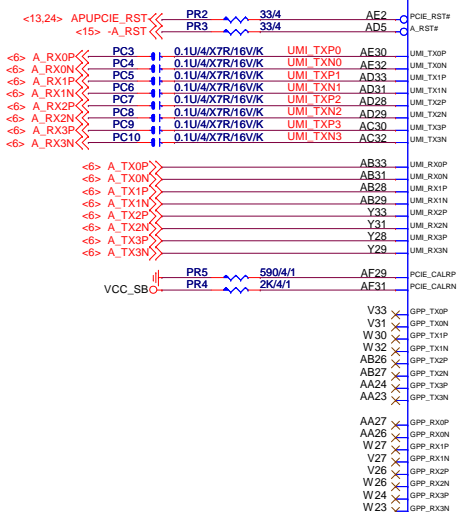
S.B HEATSINK



SB_HS[12SP2-SA0301-11R_12SP2-SA0301-12R_12SP2-SA0301-13R]



For APU PCI_E devices.

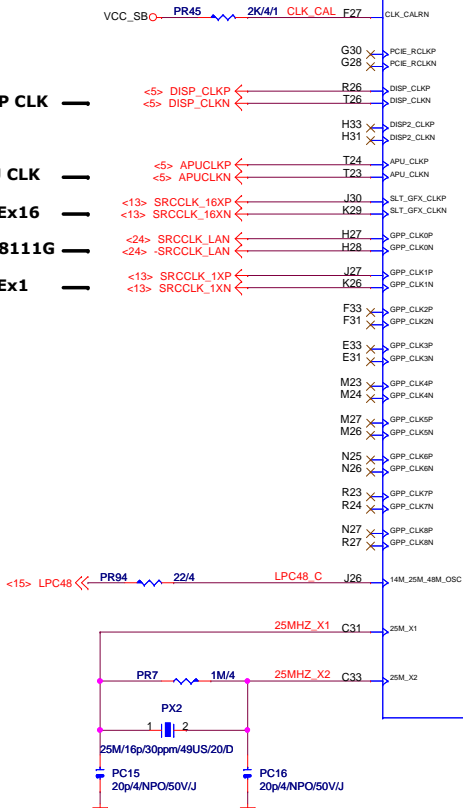


DISP CLK —

APU CLK

PCIEx16**RTL8111G**

PCIEx1

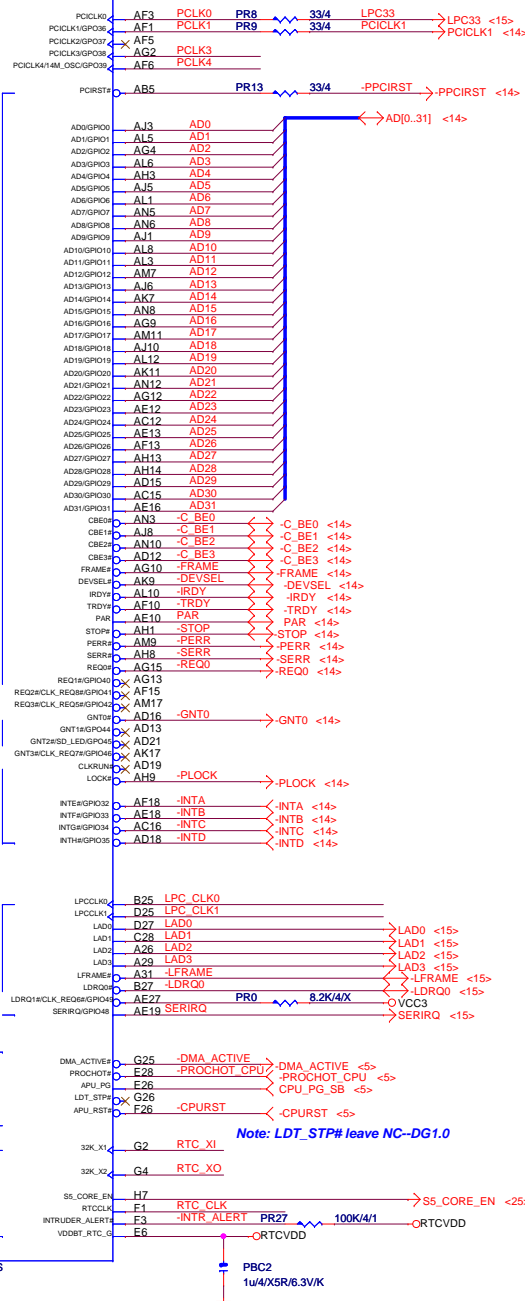


PCI EXPRESS INTERFACES

CLOCK GENERATOR

PCI INTERFACE

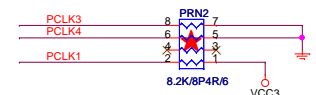
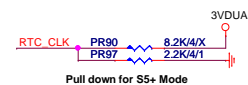
218



Note: LDT_STP# leave NC--DG1.0

→ S5_CORE_EN <25

- **PBC2**

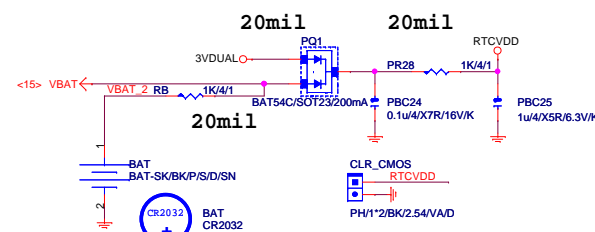


	PCLK3
PULL HIGH	USE DEBUG STRAPS
PULL LOW	IGNORE DEBUG STRAPS DEFAULT

CLKGEN Mode: Only for integrated clock mode.



	LPC_CLK0	LPC_CLK1
LL	IMC	CLKGEN
SH	ENABLED	ENABLED
	AOD Extreme	
LL	IMC	CLKGEN
W	DISABLED	DISABLED
	DEFAULT	DEFAULT



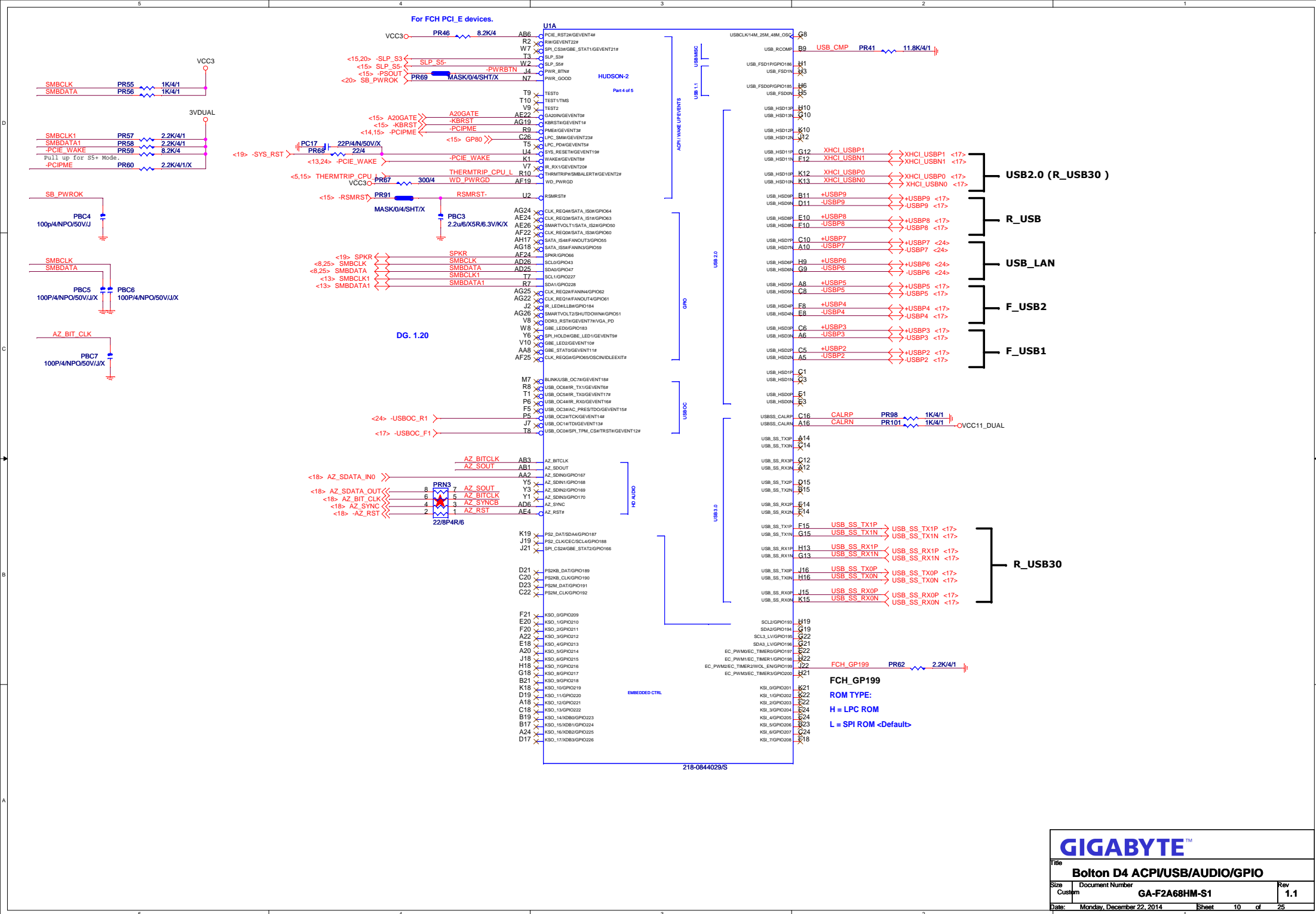
CLR_CMOS	
SHORT	CLEAR CMOS
OPEN	NORMAL

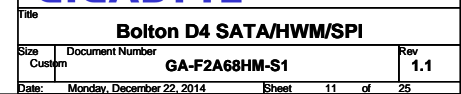
NOT ADD ICT FOR RTCVDD PIN

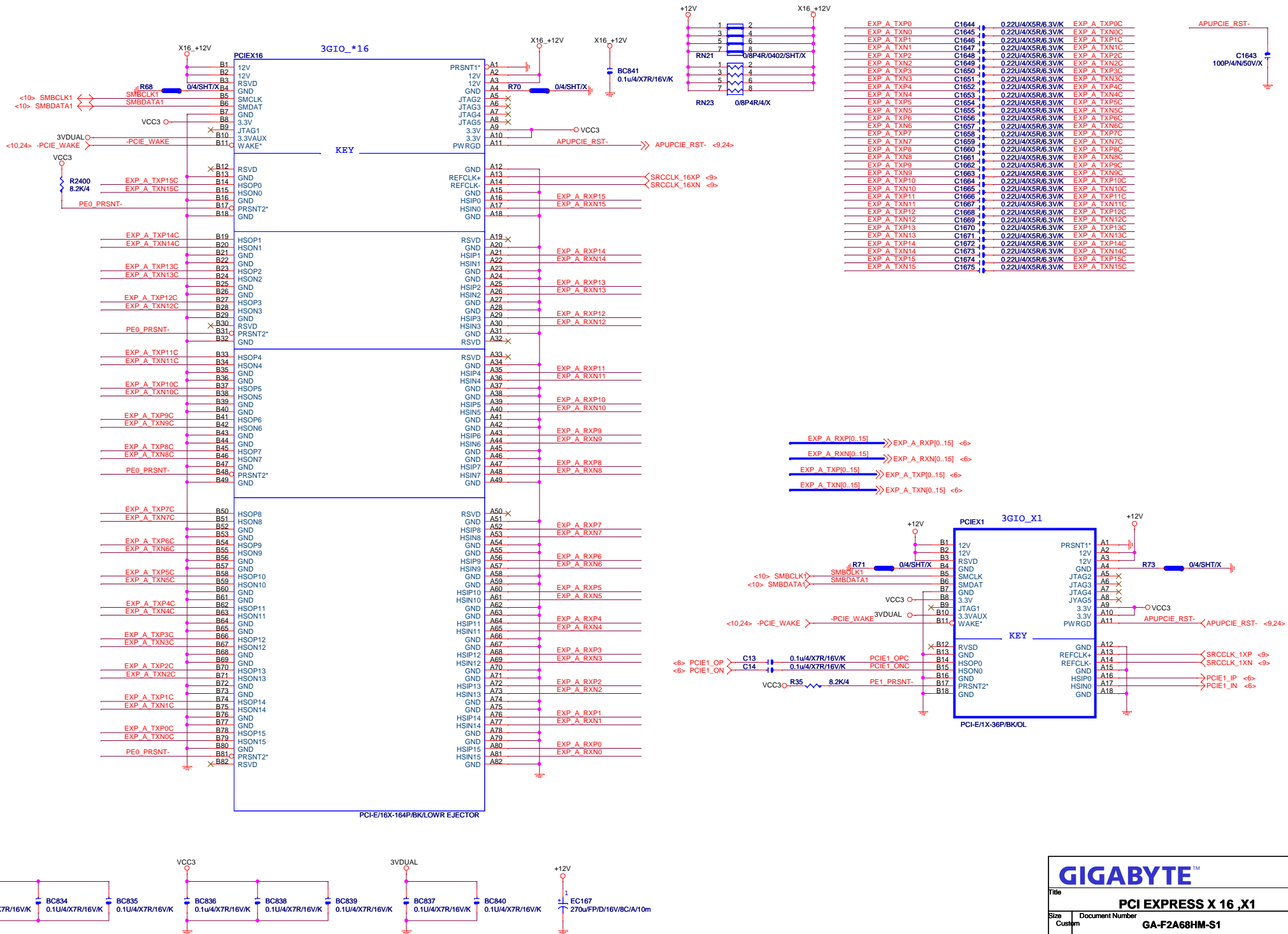
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Title	Bolton D4PCIE/PCI/CPU/LPC
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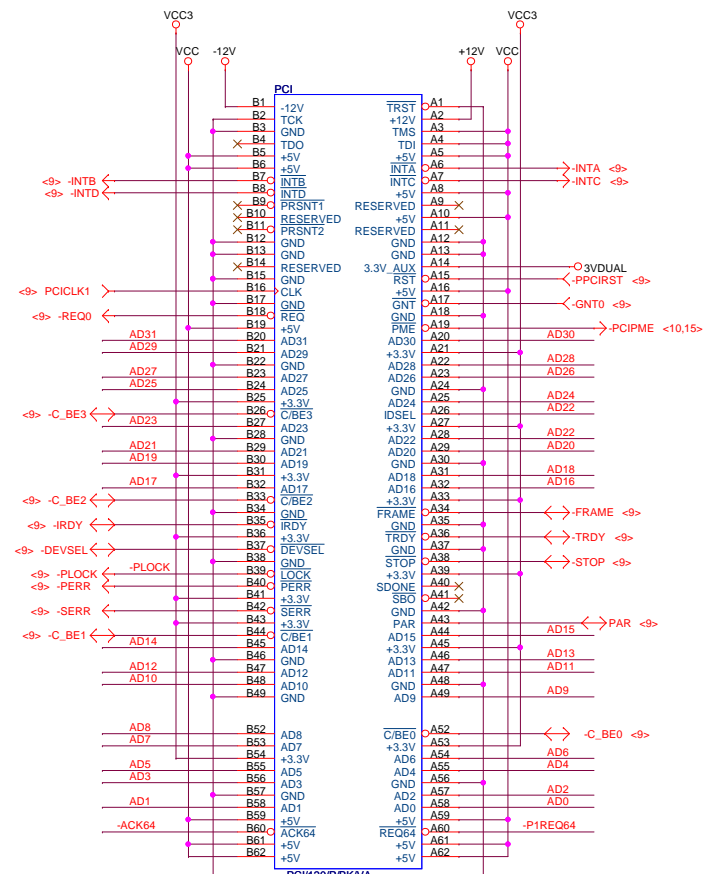




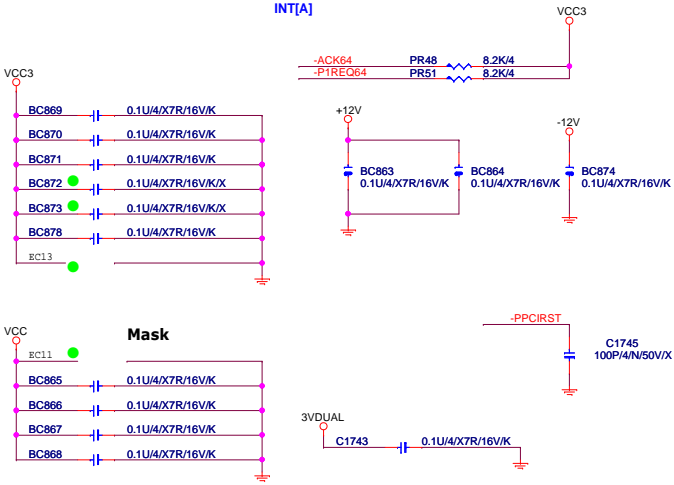


PCI SLOT 1,2

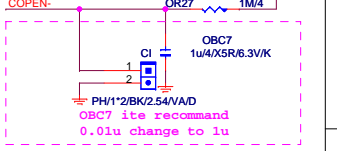
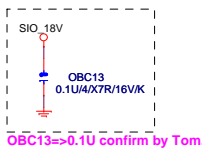
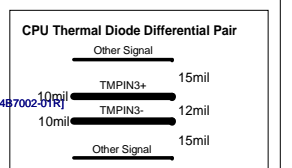
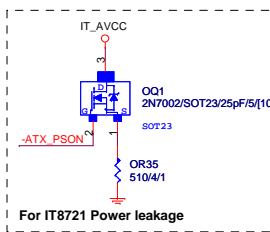
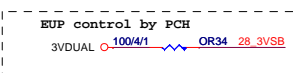
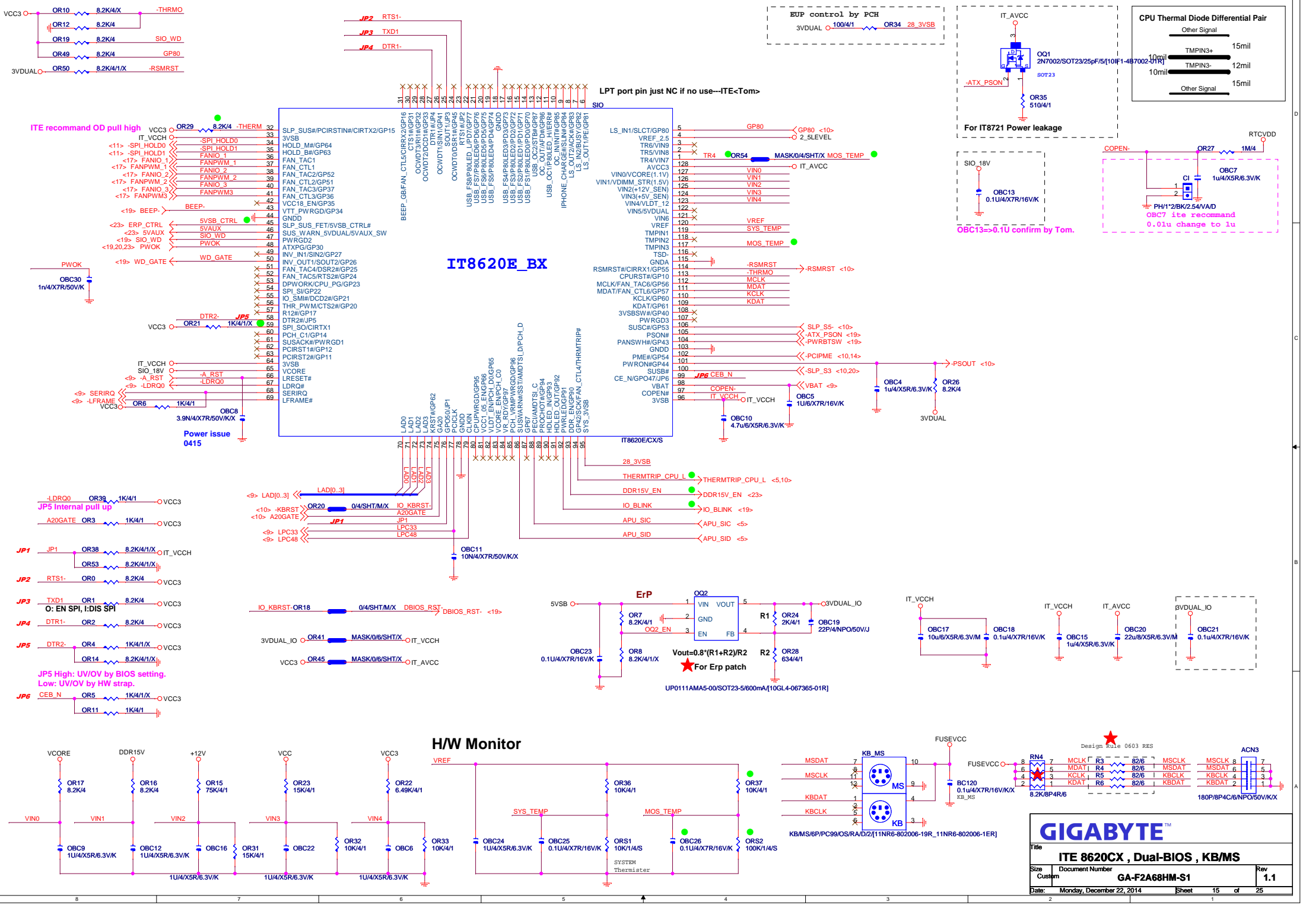
<9> AD[0..31] <-> AD[0..31]



PCI120P/BK/VA
IDSEL[AD22],
GNT/REQ[0],
INT[A]



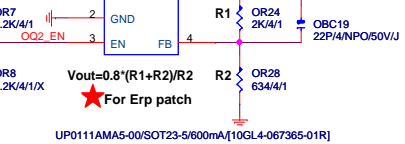
GIGABYTE™		
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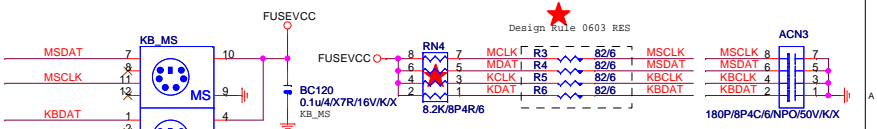
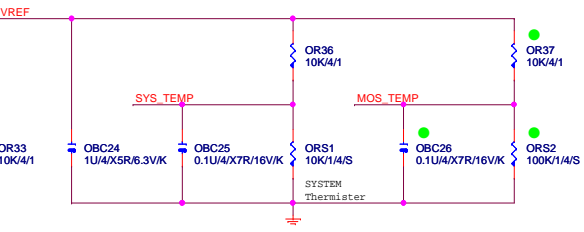
IT8620E_BX

IT8620E/CX/S

ErP



H/W Monitor



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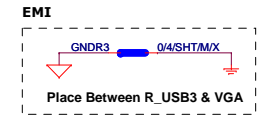
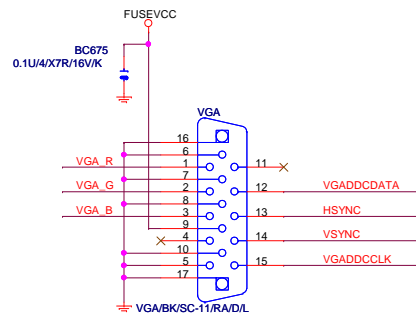
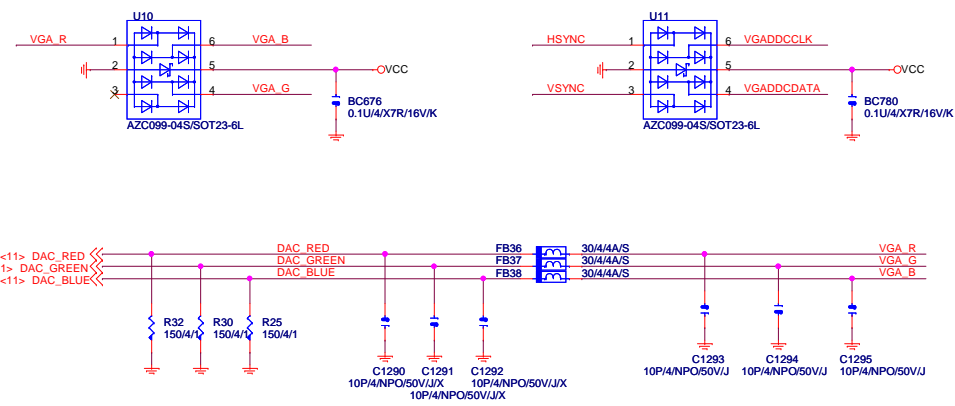
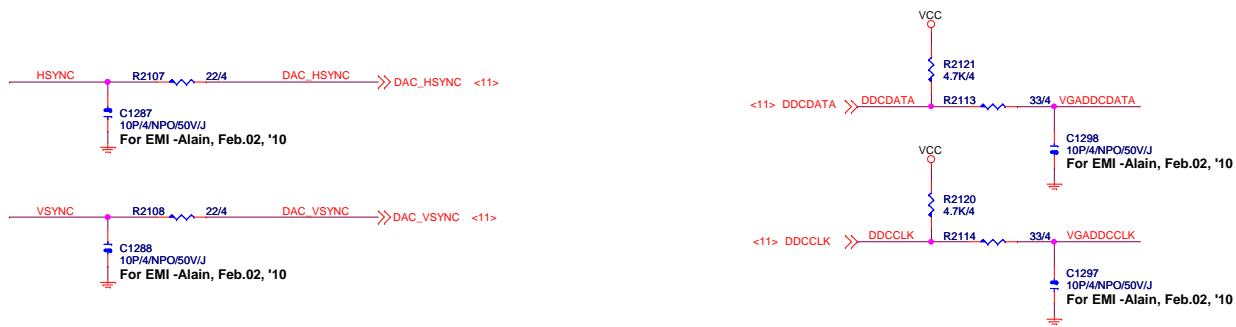
ITE 8620CX , Dual-BIOS , KB/MS

GA-F2A68HM-S1

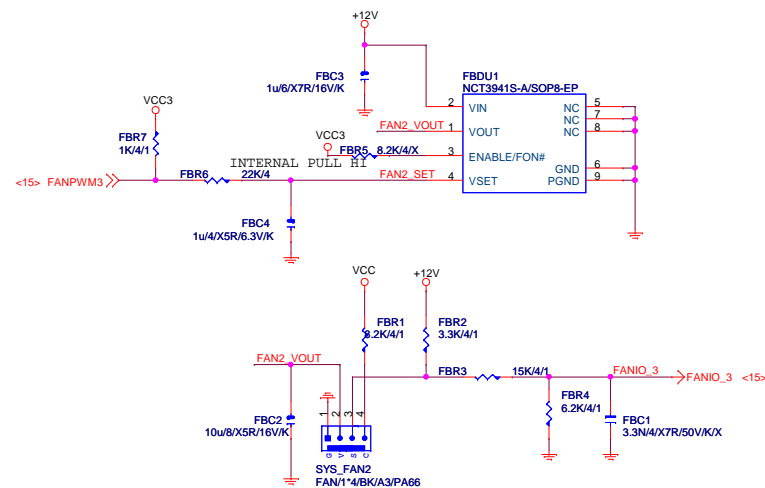
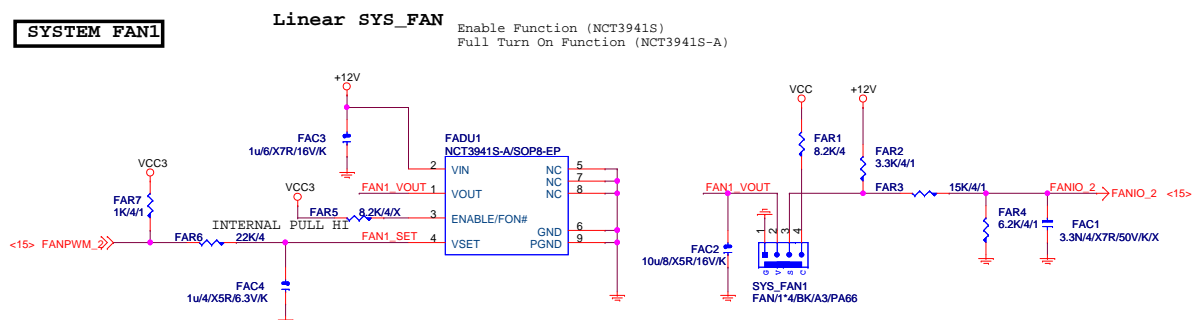
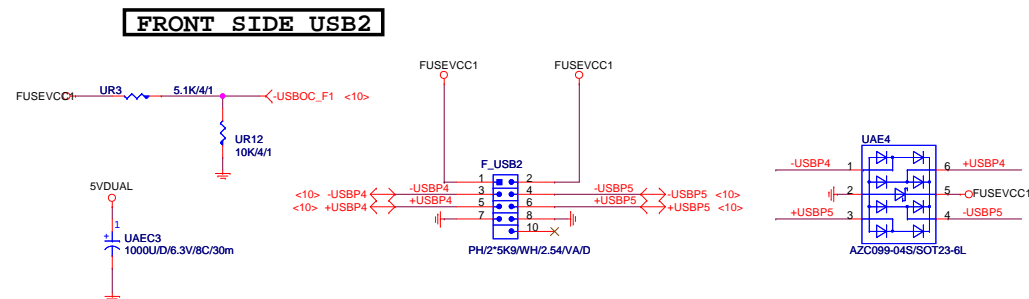
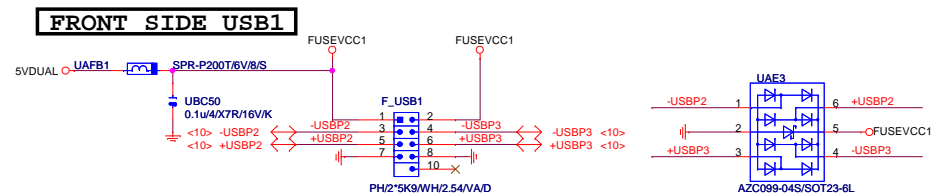
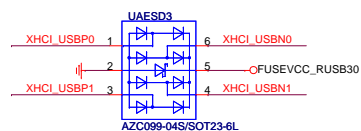
Rev 1.1

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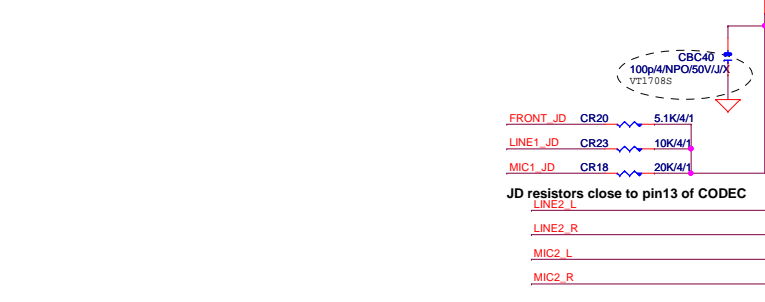
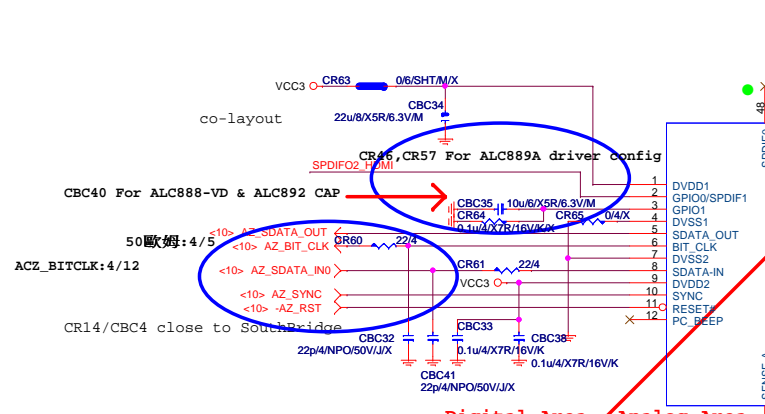
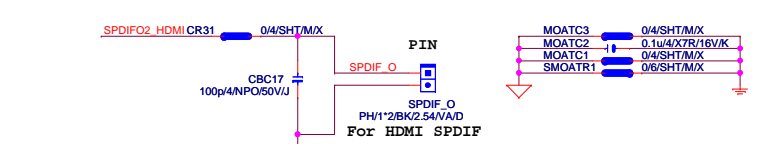
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GIGABYTE™		
RGB		
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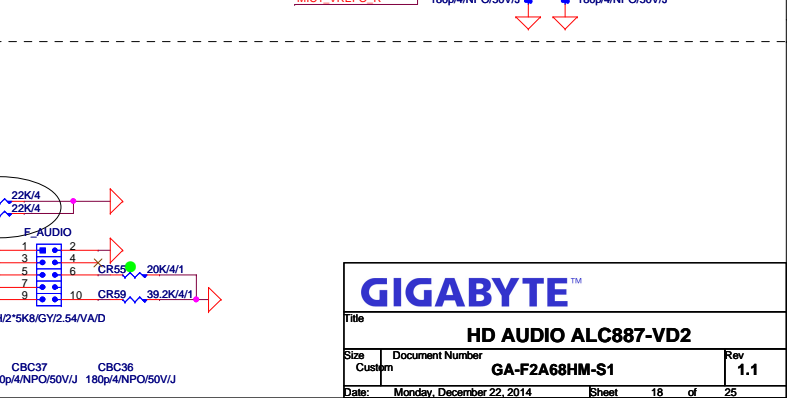
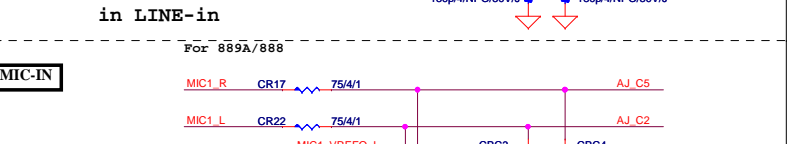
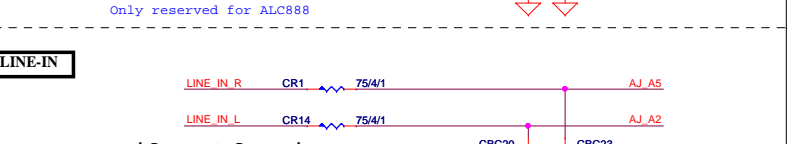
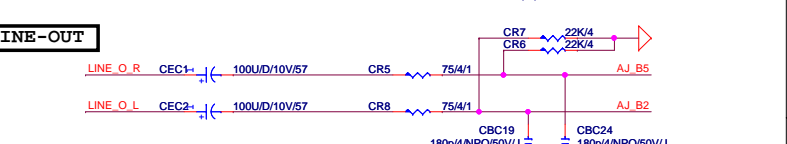
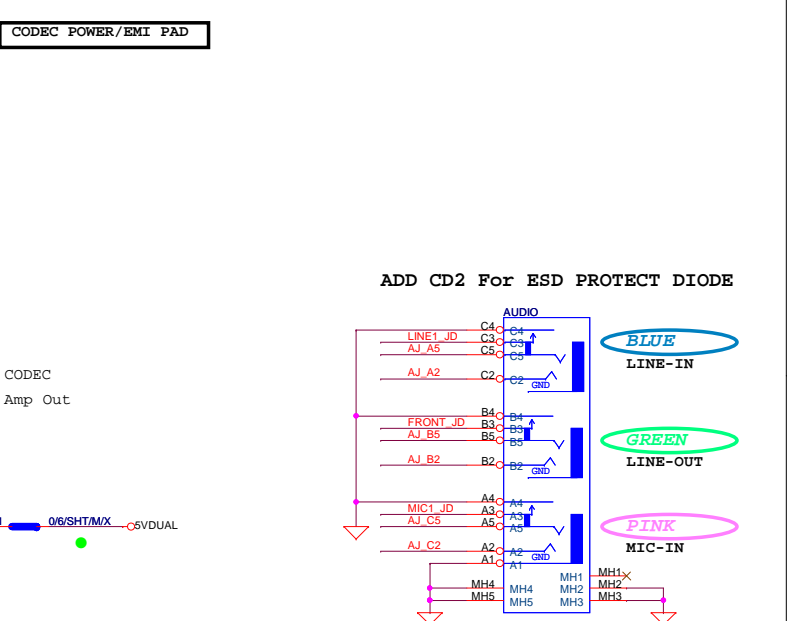
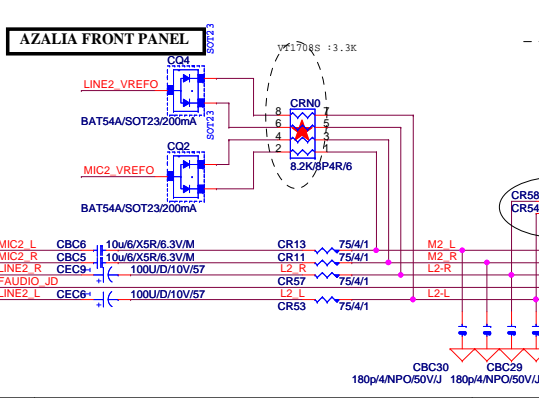
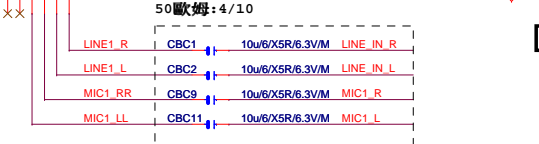
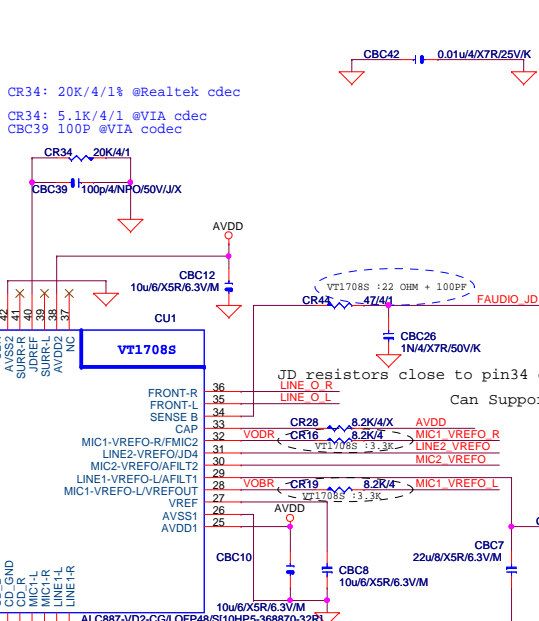


SPDIF_OUT



AZALIA CODEC ALC887-VD2/ALC889/VT1708S/VT1708SCE Colay

	ALC887-VD2	ALC889	VT1708S	VT1708SCE
CR65	X	O	O	X
CR64	X	X	X	O
CR44/CBC26	47ohm+1nF	47ohm+1nF	22ohm+100P	22ohm+100P
CR34	20K/1%	20K/1%	5.1K/1%	20K/1%
CR31	O	O	O	O
CR30	X	X	X	X
CBC1/CBC2	22uF/X5R	22uF/X5R	22uF/X5R	22uF/X5R
CR20	5.11K/4/1	5.11K/4/1	5.1K/4/1	5.1K/4/1
CBC35	O	X	X	O
CBC39/CBC40	N/A	N/A	100P/4	100P/4
CR6/CR7/CR54/CR58	22K/4	22K/4	10K/4	10K/4
CR5/CR8/CR13/CR11/CR57/CR53	75 ohm	62 ohm	75 ohm	75 ohm
CR51/CD1/CBC7	O	X	X	O
CD2/CD3/CQ3/CQ5	X	O	O	X
CR1/CR14/CR17/CR22	75 ohm	62 ohm	1K ohm	1K ohm

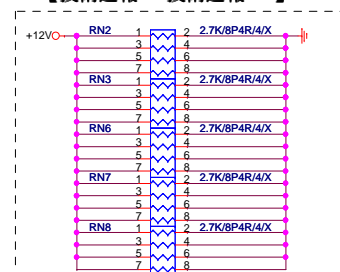
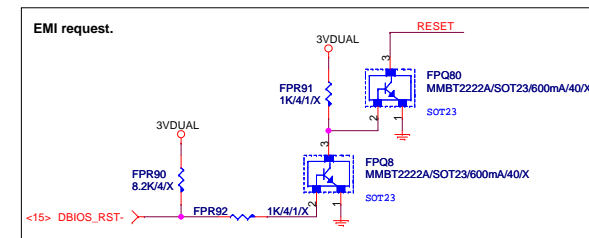
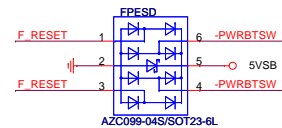


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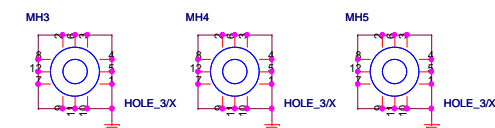
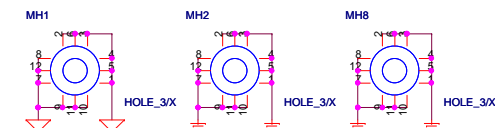
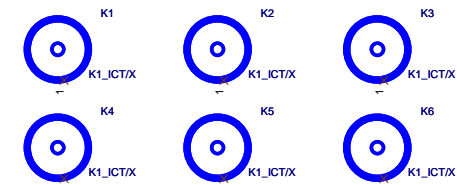
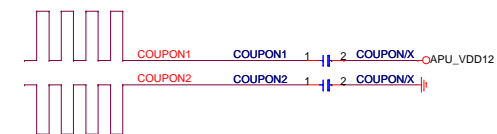
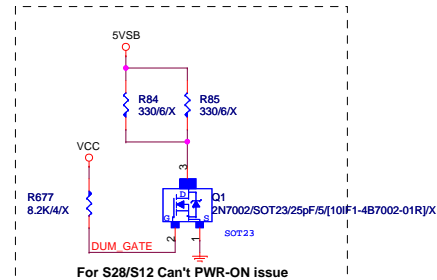
HD AUDIO ALC887-VD2

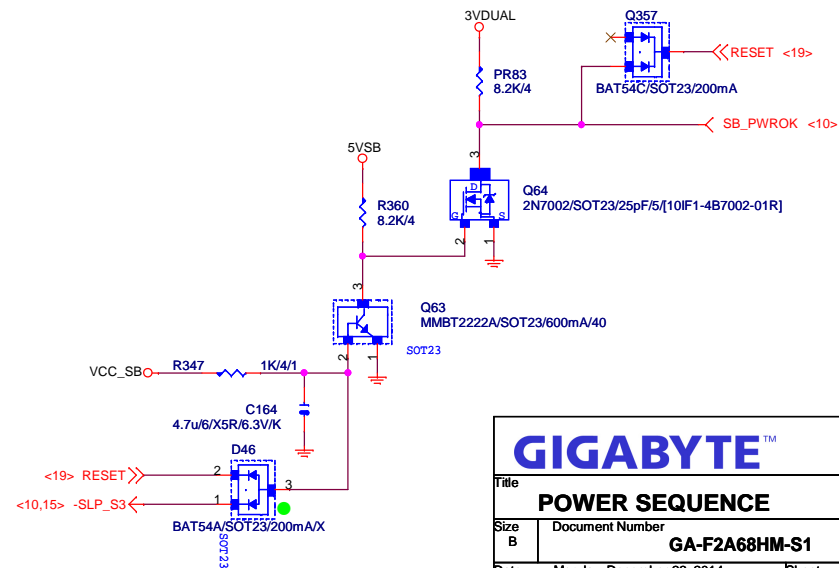
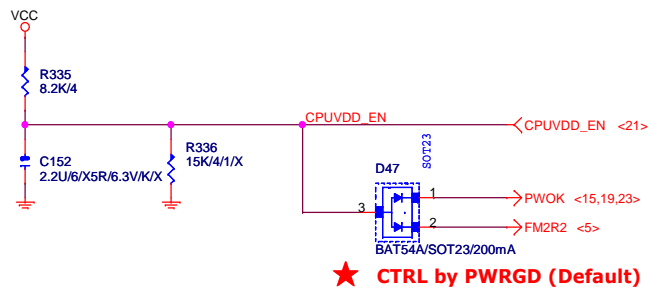
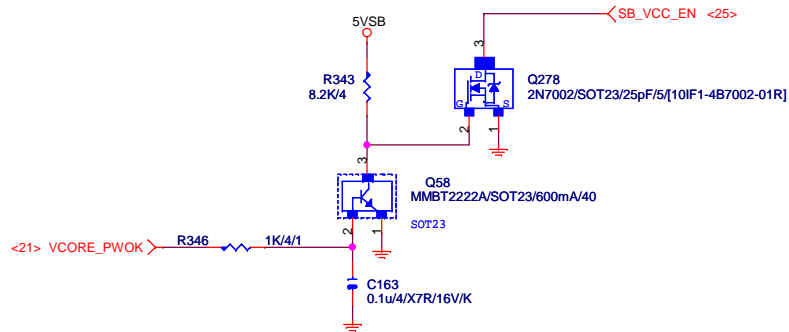
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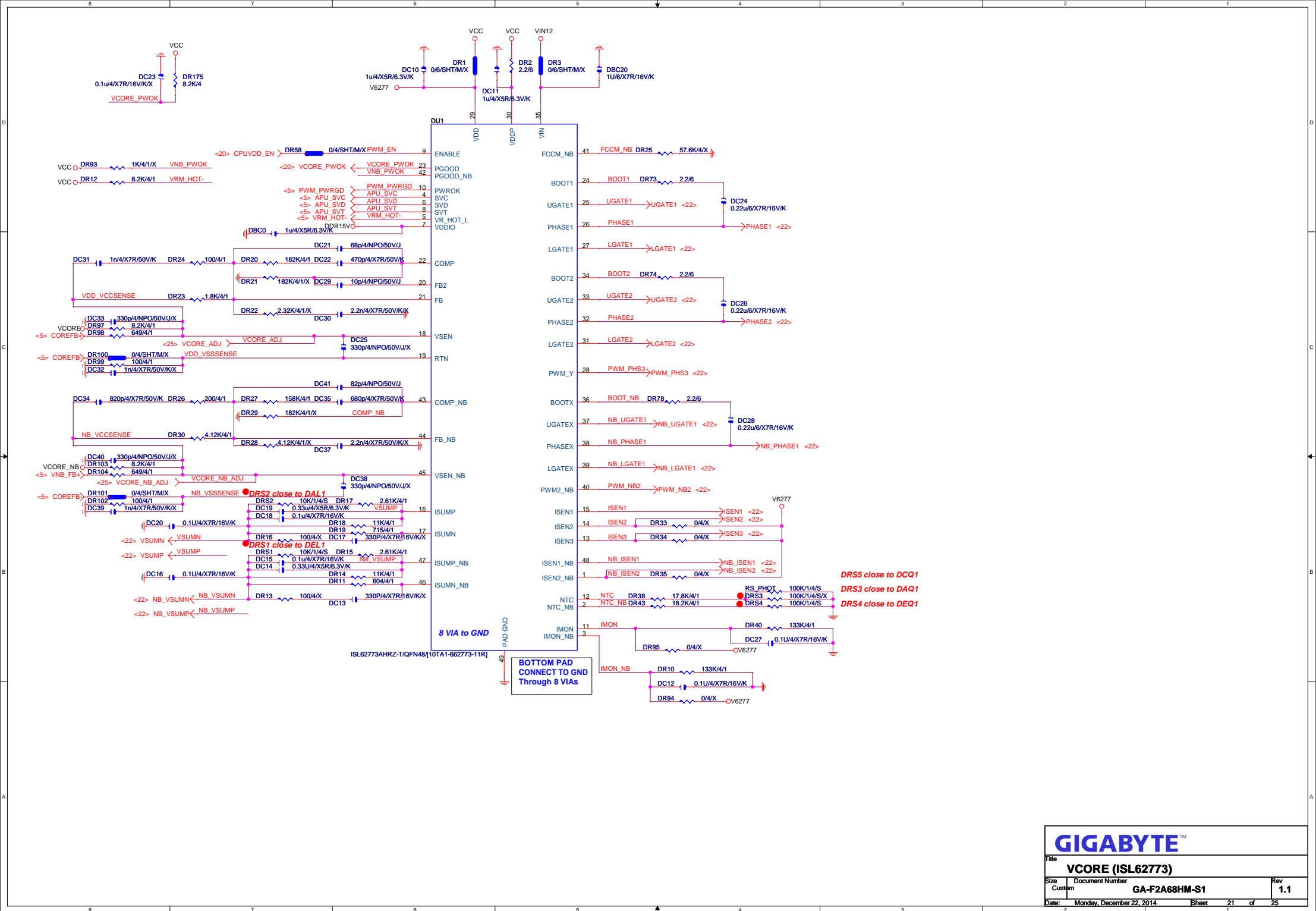


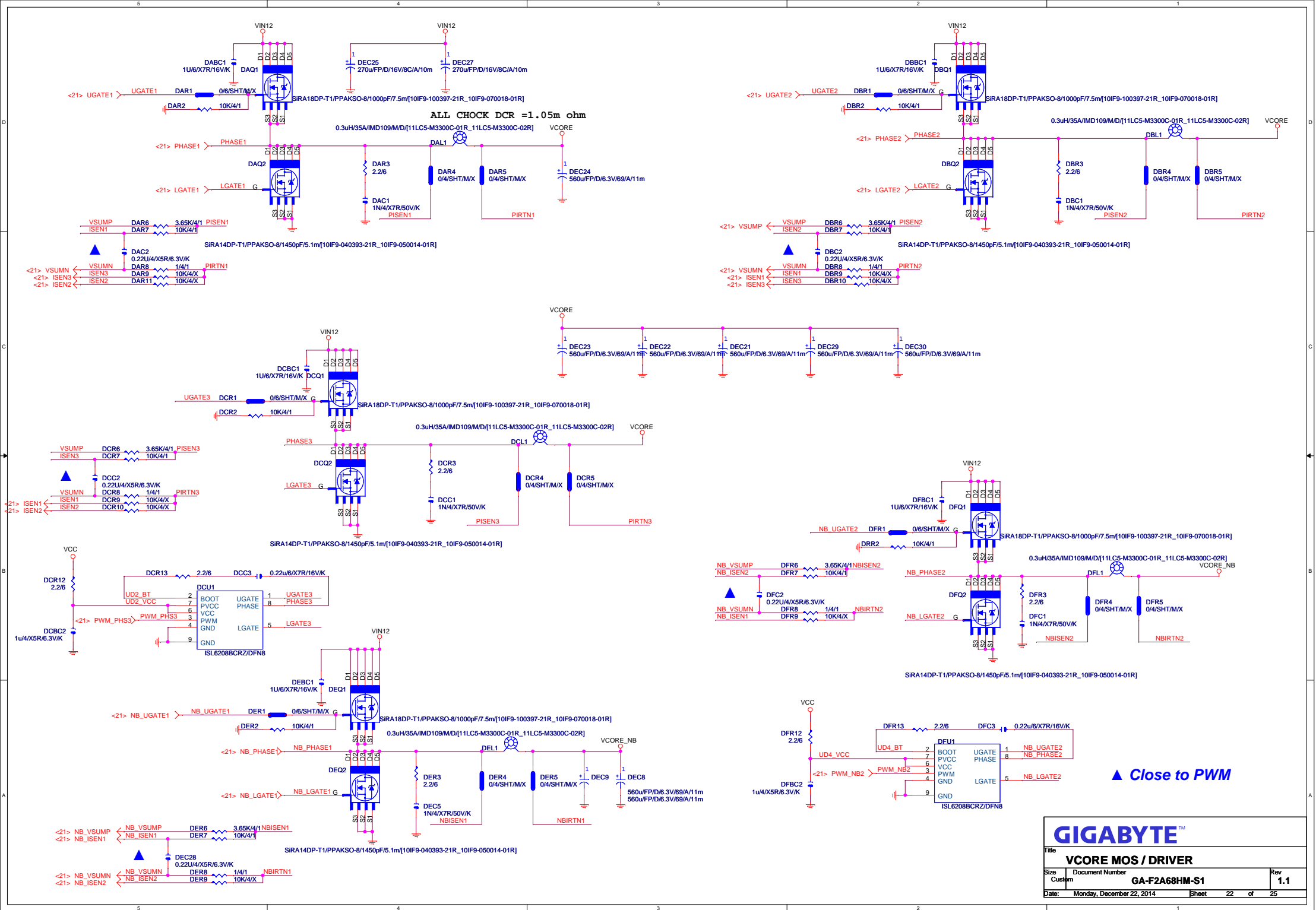
To fix 12V light load abnormal issue



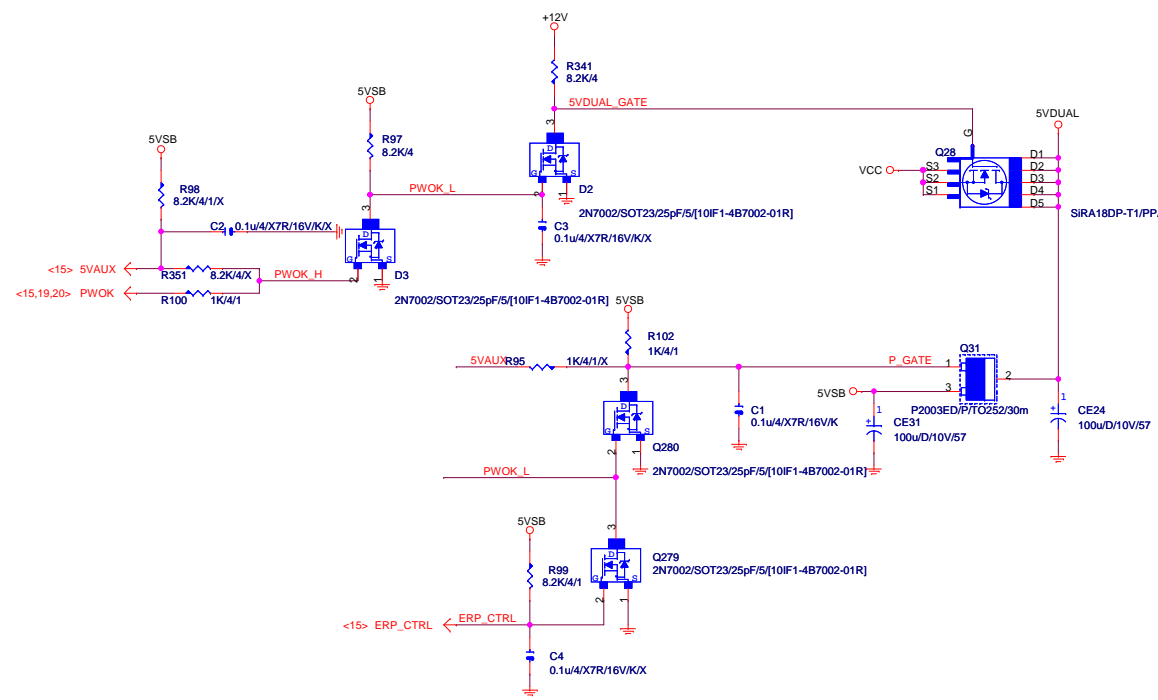


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POWER SEQUENCE			
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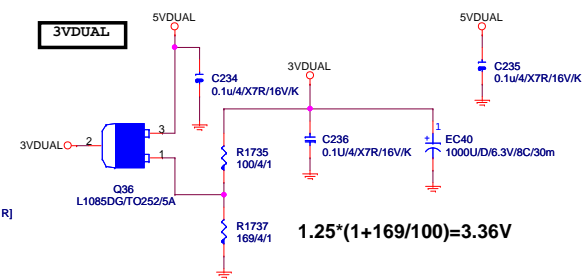




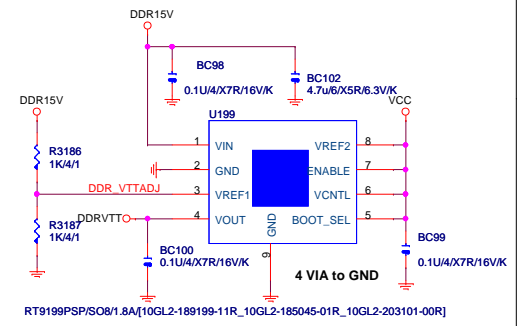
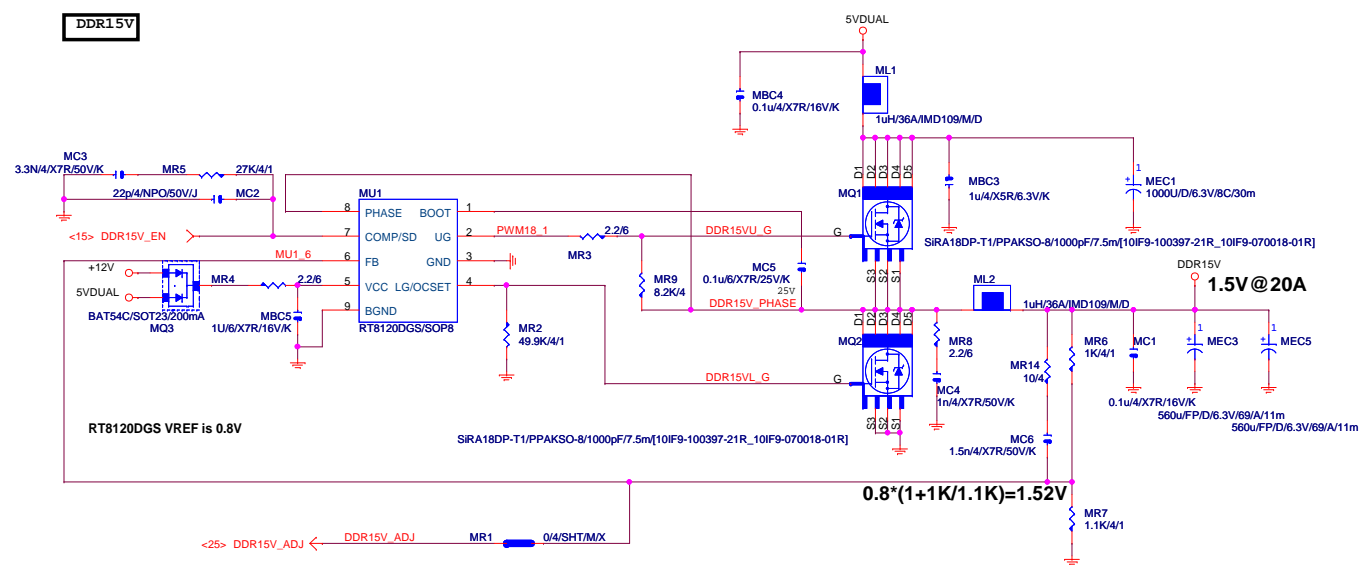
5VDUAL



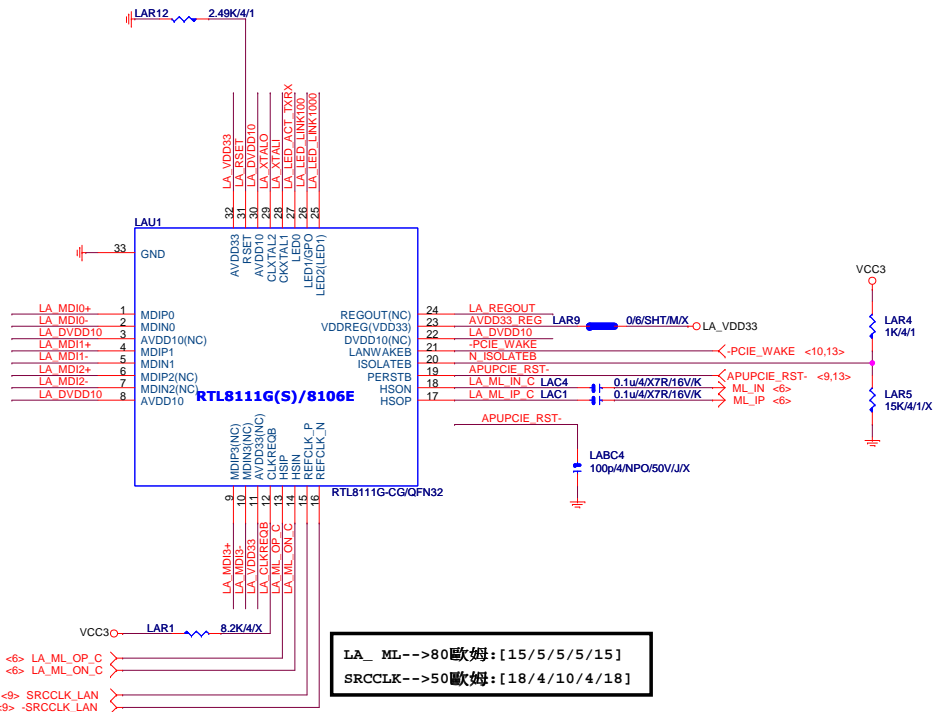
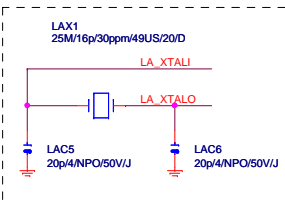
3VDUAL



DDR15V

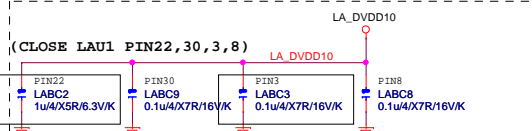


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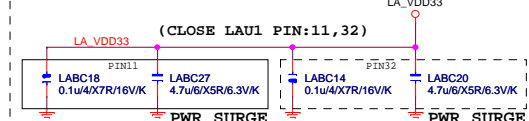
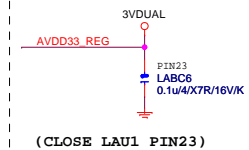


LA_ML-->80欧姆:[15/5/5/15]
SRCLK-->50欧姆:[18/4/10/4/18]

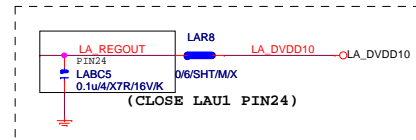
LAN POWER



LABC2:1U CLOSE PIN22[REALTEK REQ]

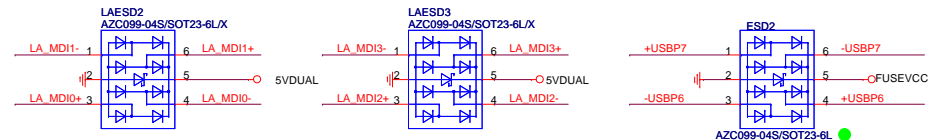


LABC18,27:CLOSE PIN11[REALTEK SURGE]
LABC14,20:CLOSE PIN32[REALTEK SURGE]

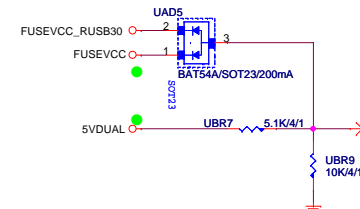
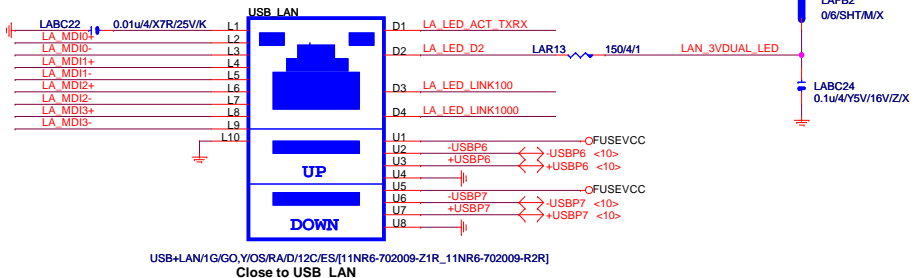


NOTE:
RT8106E:PIN3,11,22,24-->NC
LABC2LABC3,LABC5,LABC18,LABC27-->N/A

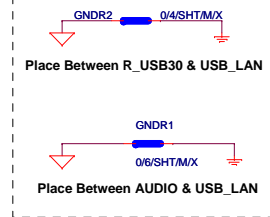
USB_LAN



USB_LAN CONNECTOR



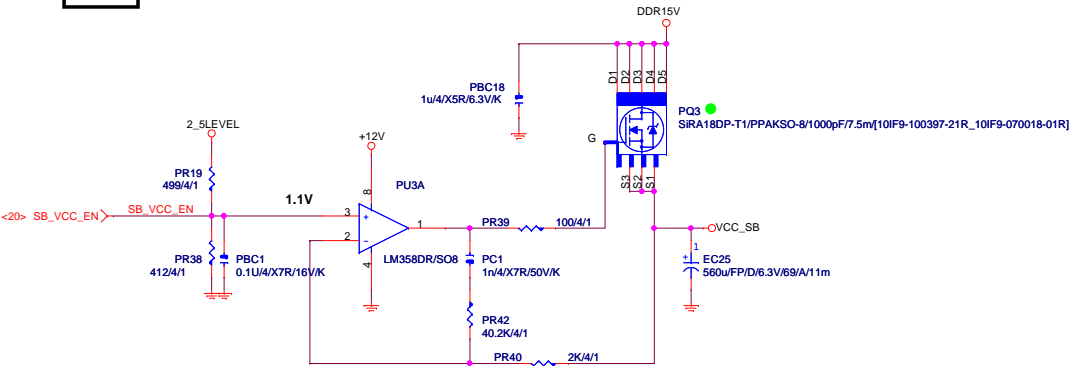
EMI



GIGABYTE™

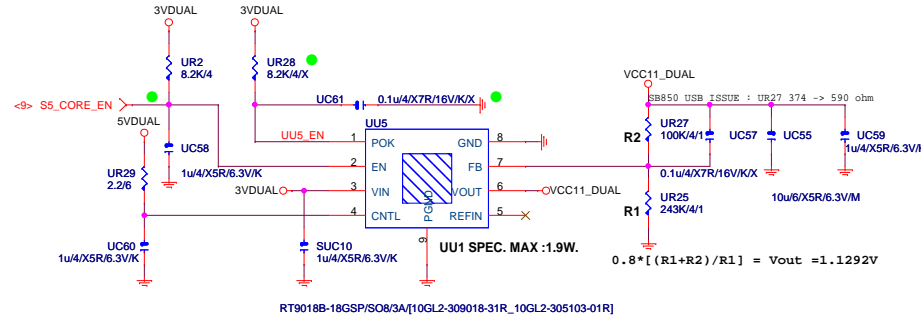
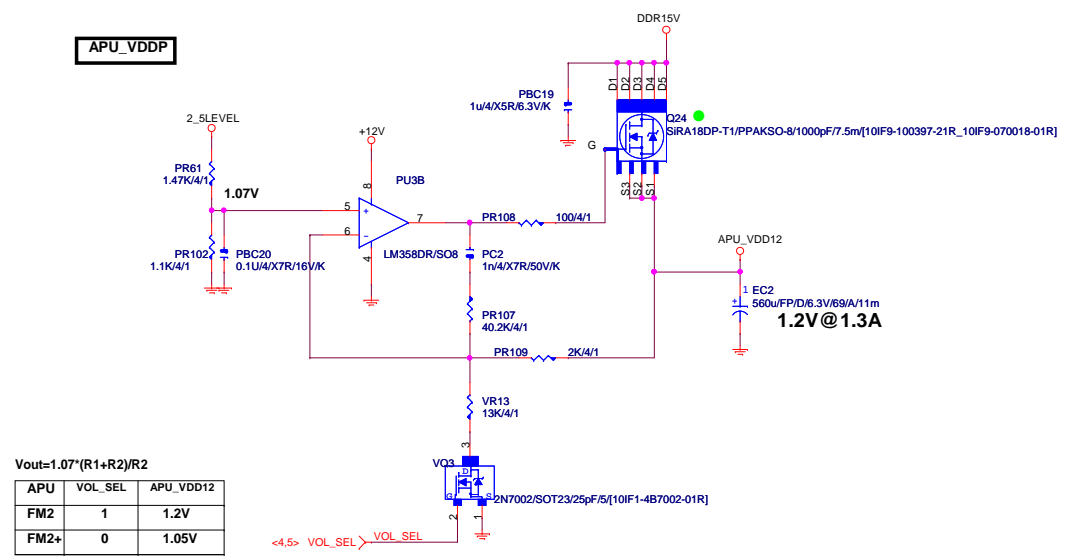
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Date	Monday, December 22, 2014	Sheet	24 of 25

VCC_SB

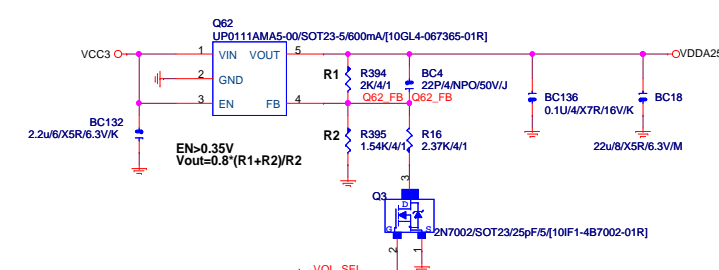
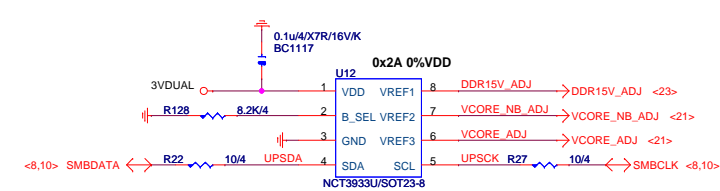


2.5LEVEL
BC0
22u/8/X5R/6.3V/M
Near PR19 / PR61

APU_VDDP



【技術通報R&D技術通報156】
RT9018 (RICHTEK) 與NCT3730 (NUVOTON),
EM5103GE (EMC) 做共用, 針對PIN7 (FB) 分壓阻值部份
(R1/R2) 須做修改為100K以上電阻值



APU	VOL_SEL	VDDA25
FM2	1	2.5V
FM2+	0	1.8V

Title
VCC_SB, APU_VDDP, VCC11_DUAL, VDDA25

Size
Custom

Date: Monday, December 22, 2014

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1.1

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